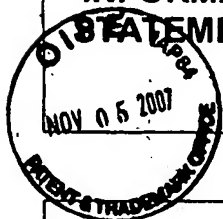


**INFORMATION DISCLOSURE
STATEMENT BY APPLICANTS
PTO-1449**



Attorney Docket No.
2885/94

Serial No.
10/526,595

Applicant(s)
Vorbach et al.

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September 8, 2003

Group Art Unit
2819

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
ll	4,233,667	November 11, 1980	Devine et al.			
	4,414,547	November 1983	Knapp et al.			
	4,720,778	January, 1998	Hansen et al.			
	4,918,440	April 17, 1009	Furtek et al.			
	5,212,716	May 1993	Ferraiolo et al.			
	5,311,079	May 10, 1994	Ditlow et al.			
	5,392,437	February 21, 1995	Matter et al.			
	5,652,529	July 1997	Gould et al.			
	5,737,516	April 1998	Circello et al.			
	5,748,979	May 1998	Trimberger			
	5,752,035	May 1998	Trimberger			
	5,841,973	November 1998	Cooke et al.			
	5,892,962	April 6, 1999	Cloutier			
	5,926,638	July 1999	Inoue			
	5,960,200	September 1999	Eager et al.			
	5,996,083	November 30, 1999	Gupta et al.			
	6,003,143	December 1999	Kim et al.			
	6,170,051	January 2001	Dowling			
	6,211,697	April 2001	Lien et al.			
	6,212,650	April 2001	Guccione			
	6,256,724	July 2001	Hocevar et al.			
	6,282,701	August 2001	Wygodny et al.			
	6,286,134	September 2001	Click, Jr. et al.			
	6,301,706	October 2001	Maslennikov et al.			
	6,398,383	June 2002	Huang, Yu-Hwei			
	6,421,809	July 2002	Wuytack et al.			
	6,425,054	July 23, 2002	Nguyen			
	6,434,695	August 2002	Esfahani et al.			
	6,434,699	August 13, 2002	Jones et al.			
	6,435,054	October 10, 2000	Nguyen			
	6,437,441	August 2002	Yamamoto			
	6,490,695	December 2002	Zagorski et al.			
	6,504,398	April 2004	Vorbach			
	6,542,844	April 2003	Hanna			
	6,757,847	June 2004	Farkash et al.			
	6,785,826	August 31, 2004	Durham et al.			
ll	6,803,787	October 2004	Wicker, Jr.			

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/94	Serial No. 10/526,595
	Applicant(s) Vorbach et al.	
	Filing Date September 8, 2003	Group Art Unit 2819

6,886,092	April 2005	Douglass et al.			
6,901,502	May 2005	Yano et al.			
6,961,924	November 2005	Bates et al.			
6,928,523	August 2005	Yamada, Akira			
2001/0010074	July 26, 2001	Nishihara et al.			
2001/0032305	October 2001	Barry			
2002/083308	June 27, 2002	Pereira et al.			
2002/0138716	September 26, 2002	Paul et al.			
2003/0056085	March 2, 2003	Vorbach			
2003/0086300	May 2003	Noyes et al.			
2003/0123579	July 3, 2003	Safavi et al.			
2003/0014743	January 16, 2003	Cooke			
2003/0192032	October 2003	Andrade et al.			
2004/0199688	October 2004	Vorbach et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	0 398 552	November 22, 1990	EPO				
	WO 94/01987	February 6, 1992	PCT				
	WO 94/08399	April 14, 1994	PCT				
	WO 99/12111	March 11, 1999	PCT				
	WO 04/114128	December 29, 2004	PCT				
	0 696 001	December 5, 2001	EPO				
	8-44581	February 16, 1996	Japan				
	7-154242	June 16, 1995	Japan				
	58-58672	April 7, 1983	Japan				
	2-226423	September 10, 1990	Japan				
	5-276007	October 22, 1993	Japan				
	8-250685	September 27, 1996	Japan				
	2-130023	May 18, 1990	Japan				
	11-307725	November 5, 1999	Japan			Abstract & Partial Translation	
	2000-181566	June 30, 2000	Japan			Computer Translation	
	9-27745	January 28, 1997	Japan			Abstract	

OTHER DOCUMENTS

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Abnous, A., et al., "The Pleiades Architecture," Chapter I of <i>The Application of Programmable DSPs in Mobile Communications</i> , A. Gatherer and A. Auslander, Ed., Wiley, 2002, pp. 1-33.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANTS
PTO-1449**

Attorney Docket No.
2885/94

Serial No.
10/526,595


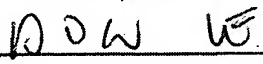
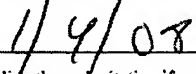
Applicant(s)
Vorbach et al.

Filing Date
September 8, 2003

Group Art Unit
2819

Alippi, et al., "Determining the Optimum Extended Instruction Set Architecture for Application Specific Reconfigurable VLIW CPUs," IEEE, 2001, pp. 50-56.
Athanas, "A Functional Reconfigurable Architecture and Compiler for Adoptive Computing," IEEE, 1993, pages 49-55
Beck et al., "From control flow to data flow," TR 89-1050, October 1989, Dept. of Computer Science, Cornell University, Ithaca, NY, pp. 1-25.
Cardoso, Joao M.P. and Markus Weinhardt, "XPP-VC: A C Compiler with Temporal Partitioning for the PACT-XPP Architecture," Field-Programmable Logic and Applications. Reconfigurable Computing is Going Mainstream, 12 th International Conference FPL 2002, Proceedings (Lecture Notes in Computer Science, Vol. 2438) Springer-Verlag Berlin, Germany, 2002, pp. 864-874.
Chen et al., "A reconfigurable multiprocessor IC for rapid prototyping of algorithmic-specific high-speed DSP data paths," IEEE Journal of Solid-State Circuits, Vol. 27, No. 12, December 1992, pp.1895-1904.
DeHon, A., "DPGA Utilization and Application," MIT Artificial Intelligence Laboratory, Proceedings of the Fourth International ACM Symposium on Field-Programmable Gate Arrays (FPGA '96), IEEE Computer Society, pp. 1-7.
Franklin, Manoj et al., "A Fill-Unit Approach to Multiple Instruction Issue," Proceedings of the Annual International Symposium on Microarchitecture, November 1994, pp. 162-171.
Hartenstein, R., "Coarse grain reconfigurable architectures," Design Automation Conference, 2001, Proceedings of the ASP-DAC 2001 Asia and South Pacific, January 30- February 2, 2001, IEEE 30 January 2001, pp. 564-569.
Hastie et al., "The implementation of hardware subroutines on field programmable gate arrays," Custom Integrated Circuits Conference, 1990, Proceedings of the IEEE 1990, May 16, 1990, pp. 31.3.1 - 31.4.3 (3 pages).
Kastrup, B., "Automatic Hardware Synthesis for a Hybrid Reconfigurable CPU Featuring Philips CPLDs," Proceedings of the PACT Workshop on Reconfigurable Computing, 1998, pp. 5-10.
Koren et al., "A data-driven VLSI array for arbitrary algorithms," IEEE Computer Society, Long Beach, CA Vol. 21, No. 10, 1 October 1988, pp. 30-34.
Lee, Jong-eun et al., "Reconfigurable ALU Array Architecture with Conditional Execution," International Soc. Design Conference (ISOOC) [online] October 25, 2004, Seoul, Korea, 5 pages.
Ling, X., "WASMII: An MPLD with Data-Driven Control on a Virtual Hardware," Journal of Supercomputing, Kluwer Academic Publishers, Dordrecht, Netherlands, 1995, pp. 253-276.
Ling et al., "WASMII: A Multifunction Programmable Logic Device (MPLD) with Data Driven Control," The Transactions of the Institute of Electronics, Information and Communication Engineers, 25 April 1994, Vol. J77-D-1, Nr. 4, pp. 309-317. [This references is in Chinese, but should be comparable in content to the Ling et al. reference above]
Ozawa, Motokazu et al., "A Cascade ALU Architecture for Asynchronous Super-Scalar Processors," IEICE Transactions on Electronics, Electronics Society, Tokyo, Japan, Vol. E84-C, No. 2, February 2001, pp. 229-237.
Razdan et al., "A High-Performance Microarchitecture with Hardware-Programmable Functional Units, Micro-27, Proceedings of the 27 th Annual International Symposium on Microarchitecture, IEEE Computer Society and Association for Computing Machinery, November 30- December 2, 1994, pp. 172-180.
Shirazi, et al., "Quantitative analysis of floating point arithmetic on FPGA based custom computing machines," IEEE Symposium on FPGAs for Custom Computing Machines, IEEE Computer Society Press, April 19-21, 1995, pp. 155-162.
Siemers et al., "The >S<puter: A Novel Microarchitecture Mode for Execution inside Superscalar and VLIW Processors Using Reconfigurable Hardware," Australian Computer Science Communications, Volume 20, No. 4, Computer Architecture, Proceedings of the 3 rd Australian Computer Architecture Conference, Perth, John Morris, Ed., February 2-3, 1998, pp. 169-178.
Skokan, Z.E., "Programmable logic machine (A programmable cell array)," IEEE Journal of Solid-State Circuits, Vol. 18, Issue 5, October 1983, pp. 572-578.
Sueyoshi, T., "Present Status and Problems of the Reconfigurable Computing Systems Toward the Computer Evolution," Department of Artificial Intelligence, Kyushu Institute of Technology, Fukuoka, Japan; Institute of Electronics, Information and Communication Engineers, Vol. 96, No. 426; IEICE Technical Report (1996), pp. 111-119 [English Abstract Only]
Weinhardt, Markus et al., "Pipeline Vectorization," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 20, No. 2, February 2001, pp. 234-248.
Weinhardt, M., "Compilation Methods for Structure-programmable Computers," dissertation, ISBN 3-89722-011-3, 1997. [TABLE OF CONTENTS AND ENGLISH ABSTRACT PROVIDED]
Xu, H.Y. et al., "Parallel QR Factorization on a Block Data Flow Architecture," Conference Proceeding Article, March 1, 1992, pages 332-336 XPO10255276, page 333, Abstract 2.2, 2.3, 2.4 - page 334.
Yeung, A. et al., "A data-driven architecture for rapid prototyping of high throughput DSP algorithms," Dept. of Electrical Engineering and Computer Sciences, Univ. of California, Berkeley, USA, Proceedings VLSI Signal Processing Workshop, IEEE Press, pp. 225-234, Napa, October 1992.

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/94	Serial No. 10/526,595
	Applicant(s) Vorbach et al.	
	Filing Date September 8, 2003	Group Art Unit 2819

	Yeung, A. et al., "A reconfigurable data-driven multiprocessor architecture for rapid prototyping of high throughput DSP algorithms," Dept. of Electrical Engineering and Computer Sciences, Univ. of California, Berkeley, USA, pp. 169-178, <i>IEEE</i> 1993.	
EXAMINER 	DATE CONSIDERED 	
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.		